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| **Student**: | Michael Escue |
| **Assignment**: | Homework #1 |
| **Class**: | ECE 351 |
| **Professor**: | Dr. Garrison Greenwood |
| **Term**: | Spring 2019 |

**Homework #1 Questions:**

**1) What is a netlist?**

A netlist is the output provided after the Register Transfer Level description is written with an HDL and processed through the Logic Synthesis Process. It’s a technology dependent description of each net which consists of the input and output wires of each module used from the vendor’s library. A netlist can be defined using VHDL, Verilog, or Circuit Reference Designators in the Electronic Design Interchange Format.

**2) Why is an HDL program technology independent?**

An HDL program describes the Register Transfer Level functionality of the design. Programmers only need concern themselves with the module function and connecting the proper net variables, not what technology the design will be fabricated with. This allows for a high level of abstraction of can easily convert between technologies with the same design.

**3) What is the purpose of simulation?**

Simulation provides a means to verify the functionality of circuits described by HDL, and Independent of fabrication technology, by applying stimulus to the design block and producing results. These results can be compared to an expected set of outputs to check if the function of the design is passing. Simulation of the design block can be instantiated within a Stimulus block where signals are directly driven into the design block, or both the stimulus block and design block are instantiated, then connect to each other within a Top-level Block for testing.

**4) Briefly describe the 3 inputs to a synthesizer.**

The three inputs to the synthesizer are the Hardware Description Language, the Design Constraints, and the ASIC Vendor Synthesis Library. Both the HDL and Constraints are technology independent but are combined with a Vendor Synthesis Library that contains technology specific components to produce the Technology-Dependent Netlist.

**5) What is a design flow?**

A design flow is the sequence of processes or requirements that lead to the implementation of a design. The design flow for developing a VLSI IC product would follow this flow:

1. Provide a Design Specification
2. Provide a Behavioral Description
3. Draft the Register Transfer Level Description in HDL
4. Perform Functional Verification and Testing
5. Complete logic Synthesis and Timing Verification
6. Obtain a Netlist
7. Perform the Logical Verification and Testing
8. Perform floor Planning and Automatic Place and Route
9. Obtain a Physical Layout
10. Verify the Layout
11. Implementation complete!

**6) What is the difference between the syntax and semantics of a program statement?**

Syntax is the set of rules for combining alphabet characters into valid program statements, whereas the semantics are the meaning of a syntactically correct program statement.

**7) Express 93 decimal as an 8-bit binary string using the Verilog syntax.**